In the Specification

Please replace the following paragraphs as indicated below. A marked-up version of each of the following paragraphs with all changes made by the current amendment shown using bracketing and underlining is attached hereto as the pages captioned "Marked-Up Specification".

Please delete the paragraph beginning at page 5, line 23 and replace it with the following:

According to a twenty-third twenty-third aspect,a system includes a scrambler that receives input and provides output; and and a switched capacitor DAC that has a plurality of capacitors and redistributes charge between at least two of the plurality of capacitors, coupled to the scrambler, that receives digital output of the scrambler.

Please delete the paragraph beginning at page 5, line 30 and replace it with the following:

According to a twenty-fifth twenty-fifth aspect of the invention, an analog to digital converter having has an analog comparison stage coupled to a digital latch stage, the analog to digital converter including a feedback element through which an output of the digital latch stage is fed back to an input of the analog comparison stage, wherein the feedback element includes a digital to analog converter.

Please delete the paragraph beginning at page 6, line 28 and replace it with the following:

According to a thirtieth aspect, in an analog to digital converter having an analog comparison stage coupled to a digital latch stage, a feedback element through which an output of the digital latch stage is coupled back to an input of the analog comparison stage, wherein the feedback element includes a digital to analog converter that receives a first multi-bit digital signal

and a second multi-bit digital signal, and produces an analog output that is indicative of a product of the first multi-bit digital signal and the second multi-bit digital signal.

Please delete the paragraph beginning at page 8, line 24 and replace it with the following:

FIG. 22 is a schematic diagram representative of another embodiment of a the DAC portion shown in FIG. 20;

Please delete the paragraph beginning at page 9, line 24 and replace it with the following:

FIG. 1 is a block diagram of one embodiment of a portion of a handset 50 for a mobile communication system. The handset 50 includes an input portion 52 having a transducer 54 that receives an input signal 56, e.g., a voice or other acoustical signal, representing information to be communicated via the mobile communication system. The transducer 54 converts the input signal 56 into an electrical signal, typically an analog signal, which is supplied to an analog-to-digital converter (ADC) 58, for example a voiceband ADC. The ADC 58 periodically samples the electrical signal and generates a sequence of multi-bit digital signals, which are supplied to a digital baseband processor 60. The baseband processor 60 performs further signal processing, including for example, compression. The output of the baseband processor 60 is supplied to burst store stage 62, which feeds a GMSK modulator 64. The GMSK modulator 64 produces multi-bit digital signals, which is supplied via signal lines, represented by a signal line 66, to a digital to analog conversion system (DAC) 68. The digital to analog conversion system 68 converts the sequence of multi-bit digital signals into an analog signal, which is supplied via signal line 70 to an output portion 72. The output portion 72 includes a mixer 72 74 that receives the analog signal on signal line 70 and feeds a transmitter 76, which in turn transmits the signal. DAC can be used in any digital to analog conversion.

Please delete the paragraph beginning at page 13, line 27 and replace it with the following:

The DAC 150 may receive a non-overlapping 3-phase clock, P1, P2, P3, shown in FIG. 3 6. The closed/open condition of the switches S3, S6, S9, and S12 is controlled by the P3 signal of

the 3-phase clock. The P1 signal of the 3-phase clock controls the open/closed condition of the charge sharing switches S13, S14, S15, and S16. The P2 signal of the 3-phase clock controls the open/closed condition of the switch S17.

Please delete the paragraph beginning at page 15, line 11 and replace it with the following:

In some embodiments, there may be one or more parasitic capacitance(s) that have an effect on the degree of correspondence, and it may be desirable, although not necessary to the techniques described herein, to provide a parasitic capacitance(s) that has an effect that offsets an effect of other parasitic capacitance.

Please delete the paragraph beginning at page 15, line 27 and replace it with the following:

In another embodiment, the digital signal bit_1, bit_2, bit_3, and bit_4 are binary-weighted bit signals. In such embodiment, the weight of the digital bit signals bit_1, bit_2, bit_3, and bit_4 are 1, 2, 4, and 8, respectively. To accommodate these various weights, each of the SC DACs utilize an amount of charge proportional to the weight of the bit signal supplied to the SC DAC. Thus, C1 is provided with ½ of the charge provided to C2, ¼ of the charge provided to C3, and 1/8 of the charge provided to C4. In other words, the charge provided to C4 is 8 times that provided to C1, 4 times that provided to C2, and 2 times that provided to C3. On clock phase P1, switches S13-S16 are in the closed condition, whereby charge is redistributed among the capacitors so that the voltage across each of the capacitors is indicative of the sum ~~each of the capacitors is indicative of the sum~~ of the values of the bits in the multi-bit signal. The charge on each capacitor is equal to the voltage across that capacitor multiplied by its ~~capacitor~~ capacitance. On the phase P2, the output switch S17 is in the closed condition and one of the capacitance delivers its charge to the output terminal.

Please delete the paragraph beginning at page 16, line 29 and replace it with the following:

Referring now to FIG. 8C, on phase P1 of the 4-phase clock, charge sharing switches S19 and S21 are in an open condition. Charge sharing switches S22 and S23 are in a closed condition, the charge on capacitor C1 of the one-bit DAC 162 is redistributed between capacitor C1 and capacitor C3 of the one-bit DAC 166. In particular, in one embodiment the charge on the capacitor C1 is divided substantially evenly between capacitor C1 and capacitor C3 such that each ends up with substantially one half of the charge on capacitor C1 in FIG. 8B, i.e., one quarter of the total charge on capacitor C1 in FIG. 8A. Referring now to FIG. 8D, on phase P2 charge sharing switches S19, S20, S21, and S23 are in an open condition. Also on phase P2 switches ~~witches~~ S18, S22, and S24, are in a closed condition whereby capacitor C1 (FIG. 5) of the one-bit DAC 162 delivers its charge to the output terminal 160.

Please delete the paragraph beginning at page 18, line 6 and replace it with the following:

Referring now to FIG. 11C, on phase P1, charge sharing switches S19 and S21 are in an open condition and charge sharing switch S26 is in a closed condition. The charge on capacitor C1 of the one-bit DAC 162 is redistributed between capacitor C1 and capacitor C3 of the one-bit DAC 166. In particular, the charge on the capacitor C1 is divided substantially evenly between capacitor C1 and capacitor C3 such that each ends up with ½ the charge on capacitor C1 in FIG. 11B, i.e., ¼ of the total charge on capacitor C1 in FIG. 11A. Referring now to FIG. 11D, on P2 charge sharing switches S19, S20, S21, S26, and S27, are in an open condition, and switches S18, and S25, are in the closed condition whereby capacitor C1 of the one-bit DAC 162 (FIG. 5) delivers its charge to the output terminal 160. Although switch S27 is in an open condition on phase P2 and does not deliver charge, in other embodiments, switch S27 may be configured to be in a closed condition on phase P2 so that switch ~~27~~ S27 delivers a copy of the charge, which is in addition to the copy delivered by switch S25. In still further embodiments, an additional clock phase, e.g., a phase P5, is provided and switch 27 is used to deliver a copy of the charge on phase P5.

Please delete the paragraph beginning at page 20, line 16 and replace it with the following:

FIG. 15 is a block diagram of another embodiment of the SC DAC 150, which is similar to the SC DAC 150 illustrated in FIGS. 9, 10A-10C, except that the SC DAC 150 of FIG. 15 further comprises ~~a switch 148, a switch 149, and a switch 150~~ a switch S48, a switch S49, and a switch S50. A first terminal of the switch S48 is connected to the second terminal of the charge sharing switch S43. A first terminal of the switch S49 is connected to the second terminal of the charge sharing switch S45. A first terminal of the switch S50 is connected to the second terminal of the charge sharing switch S46. Each of the switches S48, S49, and S50 may, but need not serve one or more of the functions noted hereinbelow. In one embodiment, one purpose of the switches S48, S49, S50 is to provide parasitic capacitance similar to that of output switch S47, so as to help cancel the effect of the parasitic capacitance of switch S47.

Please delete the paragraph beginning at page 21, line 32 and replace it with the following:

Referring now to FIG 16D, in some embodiments, the SC cell 300 is further adapted to electrically connect ~~to the SC cell 300~~ to the SC cell 300A if the SC cell 300A is positioned adjacent to the SC cell 300 and oriented such that its reference direction is directed in a direction having a predetermined angular offset from the reference direction D_{300} of the SC cell 300. In this embodiment, the predetermined angular offset is ninety degrees. In other embodiments, other predetermined angular offsets may be employed. In such position and orientation, the terminal 312 on SC cell 300 electrically connects to the terminal 311A on SC cell 300A, thereby coupling capacitor C2 of SC cell 300 to capacitor C2A of SC cell 300A through switch S48A.

Please delete the paragraph beginning at page 23, line 1 and replace it with the following:

The digital signal bit_1 and the phase P3 signal are supplied to the switch control portion 350, which generates switch control signals, on signal lines 360, 362 supplied to the SC cell 300A. The digital signal bit_2 and the phase P3 signal are supplied to the switch control portion 352, which generates switch control signals, on signal lines 364, 366 supplied to the SC cell ~~300B~~ 300B. The digital signal bit_3 and the phase P3 signal are supplied to the switch control portion 354, which generates switch control signals on signal lines 368, 370 supplied to the SC cell 300C.

The digital signal bit$_4$ and the phase P3 signal are supplied to the switch control portion 356, which generates switch control signals, on signal lines 372, 376 supplied to the SC cell 300D.

Please delete the paragraph beginning at page 24, line 18 and replace it with the following:

In this embodiment, the SC DAC 108 and the SC DAC 150 each receive a non-overlapping three phase clock. On phase P2, the one-bit DAC of the MSB of the SC DAC 108 undergoes pre-charge in accordance with the logic state of the MSB signal into the SC DAC 108. On phase P3, a charge sharing switch of the SC DAC 108 is in the closed condition, whereby ~~charge~~ the one-bit DAC of the MSB portion of the SC DAC 108 shares charge with the preceding one-bit DAC of the SC DAC 108. Also on phase P3, the SC DAC 150 undergoes pre-charge in accordance with the multi-bit digital signal, bit$_1$, bit$_2$, bit$_3$, bit$_4$. On phase P1, the charge sharing switches of the SC DAC 150 are in the closed condition, whereby charge is redistributed among the one-bit DACs in the SC DAC 150 and the one-bit DAC of the MSB of the SC DAC 108. On phase P2, switch S48 is in the closed condition, and one of the one-bit DACs of the SC DAC 150 delivers charge, i.e., a data sample, to the output terminal 120 of the DAC portion 110 of the DAC stage 86 (FIG. 3).

Please delete the paragraph beginning at page 25, line 4 and replace it with the following:

FIG. 23 is a block diagram of another embodiment of the DAC stage 86, which receives a binary-weighted multi-bit digital signal on signal lines 82. The binary-weighted multi-bit digital signal is divided into a binary-weighted LSB portion and a binary-weighted MSB portion. The LSB's are supplied to a switched capacitor (SC) DAC 108 that forms an analog signal corresponding to the value represented by the LSB's. The MSB's are supplied to a thermometer encoder 112 that converts the MSB's into an equally-weighted multi-bit digital signal. The equally-weighted multi-bit digital signal is input to a scrambler 400, and help reduce the effects of the noise and/or distortion produced by the digital to analog converter. The scrambler 400 outputs equally-weighted scrambled bits which are supplied to a switched capacitor (SC) DAC 114. The SC DAC 114 forms an analog signal corresponding to the value represented by the

equally-weighted, scrambled, multi-bit digital signal. The analog signal from the SC DAC 108 and the analog signal from the segmented SC DAC 114 are summed at 118 to form an analog signal, output on signal line 120.

Please delete the paragraph beginning at page 26, line 15 and replace it with the following:

FIG. 26 is a schematic block diagram of another embodiment of the DAC stage 86 (FIG. 3) for use in the. An MSB portion of an equally-weighted multi-bit digital signal is input to the scrambler 400, which outputs equally-weighted scrambled bits to a gating stage 420. The gating stage 420 (sixteen gating stages) further receives one of the clock phase signals, e.g., P3, and outputs gated, equally-weighted scrambled bits to a switched capacitor (SC) DAC 114. The SC DAC 114 forms an analog signal corresponding to the value represented by the equally-weighted, scrambled, multi-bit digital signal. The analog signal from the SC DAC 108 is supplied to the segmented SC DAC 114, which form an analog signal, on signal line 120, corresponding to the value represented by the multi-bit digital signal input to the DAC stage 86. Scrambler 400 further receives an input signal for example having a logic state of 1. An additional gating stage 421 receives an input signal for example having a logic state of 0. Thus there are seventeen gating stages in total.

Please delete the paragraph beginning at page 26, line 27 and replace it with the following:

In one embodiment, the DAC stage 86 (FIG. 3) (operates at a cycle rate lower than that of the SC filter stage 90, for example, the DAC stage 86 (FIG. 3) may operate at a cycle rate of 6.5 MHz and the SC filter may operate at a cycle rate of 13 MHz.

Please delete the paragraph beginning at page 27, line 16 and replace it with the following:

The output of the input op amp is valid on phase P3 and on phase P1. On phase P3, the one-bit DAC 202 and one-bit DAC 204 pre-charge in response to the logic state of bit_1 and bit_2, respectively, as described above with respect to FIG. 13. DAC stage switches S59, S60, S61, and

S62 are in the open condition. Also on phase P3, SC filter stage switches S63, S64, S68, S69, S72, and S74 are in the open condition. Switches S65, S66, S67, S70, S71, and S73 are in the open condition. On phase P4, the charge sharing switches, e.g. S59 and S60 of the SC DAC stage are in the closed condition, whereby charge is redistributed among the one-bit DACs. Also on phase P4, SC filter switches S63, S64, S68, S69, S72, and S74 are in the closed condition. Switches S65, S66, S67, S70, S71, and S73 are in the open condition, whereby the input op amp of the SC filter stage 90 undergoes offset and gain compensation. Gain compensation is most effective when the sample rate is much higher than the bandwidth of the analog signals from the DAC stage. On phase P1, switch S61 closes and one of the one-bit DACs of the SC DAC delivers charge, i.e. a data sample, to input of the SC filter stage, which in this embodiment appears as a offset and gain compensated virtual ground. Switches S59 and S60 are in the open condition. Also on P1, the SC filter stage 90 switches S67 and S70 are in the closed condition, through which the output of the SC filter stage 90 is connected back to the input of the SC filter stage 90. Switches S65, S71, and S73 are in the closed condition as well. Switches S63, S64, S68, S69, S72, and S74 are in the open condition. On phase P2, SC filter switches S62 and S63 are in the open condition thereby opening the connection between the[feedback between] output and the input of the SC filter stage 90. Switch S62 is in the closed condition whereby the one-bit DAC 202 delivers charge, i.e. a data sample, to input of the SC filter stage. Switches S61, S60, and S59 are in the open condition. Also on phase P2, switch ~~S75~~ S65 , S66, S68, S69, S72, and S74 are in the closed condition. Switches S63, S64, S67, S70, S71, S73 are in the open condition. On phase P3, switches S59, S60, S61, and S62 are in the open condition and the SC DAC undergoes another precharge in accordance with the multi-bit input signal.

Please delete the paragraph beginning at page 28, line 10 and replace it with the following:

Thus, the DAC stage delivers more than one analog signal (e.g., two analog signals in this embodiment), during each cycle of the DAC (e.g., each cycle of the four phase clock), whereby the output sample rate of the DAC matches the input sample rate of the SC filter stage. The analog signals may but need not be identical to one another. In some embodiments, the two analog signals from the DAC are not identical but the downstream stages provide appropriate

compensation ~~to~~ so that the two analog signals contribute equally to the output of the Digital to Analog Conversion System. Any type of SC DAC may be used so long as the DAC generates suitable "copies" of the analog signal. In some embodiments, a SC DAC of the type shown in FIG. 18 and 19A-19C may be used because it can inherently provide multiple copies of the output signal.

Please delete the paragraph beginning at page 28, line 24 and replace it with the following:

There are many ways to physically arrange the stages in each of the figures. For example, in one embodiment, one gate stage is integrated into each of the SC cells in order to reduce the number of data lines that are routed to the DAC stage. In another ~~Another~~ embodiment, the gate stages are integrated near the scrambler cell in order to reduce the size of the SC cells.

Please delete the paragraph beginning at page 28, line 30 and replace it with the following:

In some embodiments, the value of the capacitance used in the SC DAC may be selected so as to be large enough to meet bit weight matching requirements. However, these are just two example criteria. The criteria for selecting the value(s) of the capacitance used in the SC DAC are not limited to those of noise requirements and/or bit weight matching requirements.

Please delete the paragraph beginning at page 30, line 8 and replace it with the following:

FIG. 28B is an illustration of a top view of another embodiment of a SC cell 450 implementing the one-bit DAC of FIG. 16A. This embodiment is substantially the same as the embodiment of FIG. 28A but further includes a switch S43A that is electrically in parallel with S43 and physically oriented substantially perpendicular to S43; and further includes a switch S48A that is electrically in parallel with S48 and physically oriented perpendicular to S48. For example, the switches S43, S43A may have a longitudinal axis, and the switches may be oriented such that the longitudinal axis of one switch is physically perpendicular to the longitudinal axis of

the other switch. In one embodiment, the switches S43 and ~~S43~~ S43A are formed of two switches
of approximately equal size.

Please delete the paragraph beginning at page 30, line 31 and replace it with the following:

FIG. 30 is a schematic diagram of one embodiment of the CT filter stage 92 of FIG. 2,
which includes a two resistors R600, R601 that each receive an analog signal from the SC filter
stage, and form an RC filter with C600 and C601,to passively filter the images left by the
switched capacitor filter. The images ~~which~~ appear at multiples of the SC filter sample rate. The
stage may have selectable gain formed by an amplifier 600 and resistors R602-R607. The CT
filter stage may further provide resistors R608, R609, which form a passive pole in combination
with an off-chip capacitor C602. Although not required, the resistors in the output pole may be
integrated to improve I/Q channel matching, reduce external component count and to reduce the
effects of loading from the pin capacitance on the output stage amplifier.

Please delete the paragraph beginning at page 32, line 18 and replace it with the following:

FIGS. 34A-34C are block diagrams showing the operation of the squaring circuit 500 of
FIG. 31 for each of the 3 clock phases in the event that input terminals 512, 514, 516, 518 are
supplied with digital bit signals bit_1, bit_2, bit_3, bit_4, having logic states of 1, 1, 0, 0, respectively.
Tables show the relationship between the clock phase, and the state (i.e., voltage and charge) of
the capacitors in the one-bit DACs. Referring now to FIG. 33A, on phase P3 of the 3-phase
clock, all of the charge sharing switches S200, S201, S202, and S203 and the output switch S204,
are in the open condition. The capacitor C1 and the capacitor C2 are each charged to V_{ref} in
response to the logic state 1 on terminal 512 and 514, respectively. Capacitors C3 and C4 are all
discharged to ground in response to the logic 0 signals on terminals 516, 518, respectively.
Referring now to FIG. 34B, on phase P1, all of the charging switches S3, S6, S9 and S12 (FIG.
31) and the output switch S204 are in an open condition, and all of the charge sharing switches
S200, 201, 202, 203 are in a closed condition, whereby charge is redistributed and resulting in the
total charge on all of the capacitors being divided among all of the capacitors. If the capacitors

C1, C2, C3, C4 all have the same capacitance value C, then the charge is shared equally so that the voltage across each capacitor becomes $V_{ref}/2$. Referring now to FIG. 33C, ~~onl~~ <u>on</u> P2 of the 3-phase clock, switch S200 is in the closed condition because P2 has a logic state 1 and bit_1 has a logic state 1. Switch S201 is in the closed condition because P2 has a logic state 1 and bit_2 has a logic state 1. Switches S202, S203 are in the open condition because bit_3, bit_4 have a logic state 0. Output switch S204 is in the closed condition, and capacitors C1 and C2 (FIG. 31) of one-bit DACs 162, 164 delivers charge to the output terminal 510. Consequently, the total charge delivered to the output terminal 510 is equal to C*Vref.